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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,101	10/23/2003	Bruce E. Hayden	520D3183	6588

7590 06/16/2006

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EXAMINER	
BONURA, TIMOTHY M	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,101	HAYDEN ET AL.	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Finch, et al, U.S. Patent Number 5,524,208.

3. Regarding claim 1:

a. Regarding the limitation of "a first register; a means for decoding a Wait for Change instruction," Finch teaches a method for waiting until a specified location in a memory ceases to have a certain value (col. 2, lines 44-60 in Finch teach that in a write-through cache design a snoop process is preformed to ensure that data stored in main memory that is also stored in cache does not changed by snooping writes by other bus masters to detect when data stored in main memory that is also stored in cache is changed by another bus master.

b. Regarding the limitation of "a means for executing a Wait for Change instruction in response to decoding the Wait for Change instruction, wherein: execution of the Wait for Change instructions terminates when either a contents of a specified location in a memory differs from a contents of the first register or a specified time period has elapsed," Finch discloses a system that upon determining that another bus master has written over data in a location in main memory containing data that is also stored in cache memory, the cache system invalidates the respective line; Note: since the cache memory invalidates the respective line after the test for determining a change in data

stored in main memory that is also stored in cache is performed the system must inherently wait for a cache invalidate signal in order to invalidate the respective line). (col. 2, lines 44-60).

4. Regarding claim 2:

c. Regarding the limitation of "a means for comparing the specified location in the memory to the contents of the first register," Finch teaches the testing in step (A) comprises: 1) comparing the contents of the specified location in the memory against a register (in col. 3, lines 24-35, Finch teaches that a snoop cycle includes a tag compare cycle).

d. Regarding the limitation of "a means for receiving a cache invalidate signal; a means for waiting for the cache invalidate signal for a cache line that includes the specified location in the memory when the comparing in means (1) fails," Finch discloses a system wherein indicating that step (A) failed when the contents of the specified location in the memory matches the contents of the register (in col. 3, lines 24-35, Finch teaches the controller latches the address during a tag compare cycle; Note: a latch is a register and a latching operation is performed by a latch).

5. Regarding claim 3:

e. Regarding the limitation of "a means for decoding a Lock instruction," Finch teaches a method for waiting until a specified location in a memory ceases to have a certain value (col. 2, lines 44-60 in Finch teach that in a write-through cache design a snoop process is preformed to ensure that data stored in main memory that is also stored in cache does not changed by snooping writes by other bus masters to detect when data stored in main memory that is also stored in cache is changed by another bus master.

f. Regarding the limitation of "a means for executing a Lock instruction in response to decoding the Lock instruction, wherein: execution of the Lock instructions terminates when either a lock value is written to a specified location in a memory overwriting a non-lock value in the specified location or a specified time period has elapsed," Finch discloses a system that upon determining that another bus master has written over data in a location in main memory containing data that is also stored in cache memory, the cache system invalidates the respective line; Note: since the cache memory invalidates the respective line after the test for determining a change in data stored in main memory that is also stored in cache is performed the system must inherently wait for a cache invalidate signal in order to invalidate the respective line). (col. 2, lines 44-60).

6. Regarding claim 4:

g. Regarding the limitation of "a means for testing the specified location in the memory for containing the non-lock value; a means for writing the lock value to the specified location in the memory when the specified location in the memory contains the non-lock value," Finch teaches the testing in step (A) comprises: 1) comparing the contents of the specified location in the memory against a register (in col. 3, lines 24-35, Finch teaches that a snoop cycle includes a tag compare cycle).

h. Regarding the limitation of "a means for receiving a cache invalidate signal; a means for waiting for the cache invalidate signal for a cache line that includes the specified location in the memory when the testing in means (1) fails," Finch discloses a system wherein indicating that step (A) failed when the contents of the specified location in the memory matches the contents of the register (in col. 3, lines 24-35, Finch teaches the controller latches the address during a tag compare cycle; Note: a latch is a register and a latching operation is performed by a latch).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

8. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

9. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

11. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

12. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER

tmb
June 08, 2006